

# A 5Gb/s Automatic Sub-Bit Between-Pair Skew Compensator for Parallel Data Communications in 0.13 $\mu$ m CMOS

Yuxiang Zheng<sup>†‡</sup>, Jin Liu<sup>†</sup>, Robert Payne<sup>‡</sup>, Mark Morgan<sup>‡</sup>, and Hoi Lee<sup>†</sup>

<sup>†</sup>University of Texas at Dallas, Richardson, TX 75080, <sup>‡</sup>Texas Instruments Inc., Dallas, TX 75243

E-mails: yuxiang@ti.com and jinliu@utdallas.edu

## Abstract

A between-pair skew compensator for parallel data communications is presented. It can detect time skew between two independent data sequences using continuous-time correlations and then automatically align the two using a voltage controlled wide-bandwidth data delay line. A 5Gb/s sub-bit between-pair skew compensator in 0.13 $\mu$ m CMOS occupies 0.03mm<sup>2</sup> active die area and dissipates 22.5mW.

## Introduction

Parallel links are widely used in high-performance computing systems to enable high-throughput data communications. However, mismatches between channels can cause data transmitted in one channel to arrive at a different time compared with that in another channel. This is referred as between-pair skew (BPS) or inter-pair skew. BPS can significantly reduce the receiver timing margin and limit the data transmission rate. To achieve a higher per pin data transmission rate, either restrictions on channel matching (which limits transmission distance or requires high-cost high-quality transmission media) are enforced to reduce BPS or per channel clock & data recovery (which consumes large power and area) is required. To avoid these issues, previous designs [1-3] have used one local core clock to generate multiple phases. For each channel, the individual clock phase is determined during a calibration period when clock signals are sent along all data lines as training signals. Additional circuit, i.e. additional power, is then needed to align recovered data from all channels. This paper presents a BPS compensator that can automatically detect skew between two independent data sequences and align the two. With the proposed compensator, a single clock recovered from a reference channel can be used to directly sample all data channels and recovered data from all channels are naturally aligned.

## Circuit Design

Fig. 1 presents the proposed automatic BPS compensation scheme. It addresses sub-bit BPS compensation only, as the integral-bit BPS portion can be compensated in a higher communication layer. The compensator includes a continuous-time voltage controlled data delay line (VCDDL) for data de-skew. It also includes a BPS detector to detect skew and generate an appropriate feedback control voltage  $V_{ctrl}$  for the VCDDL. The reference channel can be a clock or a data sequence.

Fig. 2 presents the differential VCDDL design. Since data signals have much wider bandwidth compared with clock signals, the VCDDL needs to provide a flat magnitude response and tunable group delay across the major signal spectrum to avoid distortion when delaying data signals. Wide-bandwidth delay elements have been previously studied as delay units for tap delay lines in continuous-time FIR equalizers [4, 5]. However, varying the group delay inevitably

results in a change in magnitude. In this application, it is desirable to have a delay element that maintains its magnitude when its group delay is adjusted. The proposed VCDDL consists of six cascaded differential delay elements (DE) to provide a maximum 200ps tunable delay for data in order to achieve a full sub-bit BPS compensation for 5Gb/s data. Each DE has a fast path ( $-g_{m1}$  with  $R_1C_1$ ) and a slow path ( $-g_{m2}$  with  $R_2C_{var}$  followed by  $-g_{m3}$  with  $R_1C_1$ ). The  $R_2C_{var}$  term is intended to provide adjustable delay and is much larger than  $R_1C_1$ . The magnitude of the DE transfer function  $H(\omega)$  is only determined by  $R_1C_1$  as magnitudes of  $1 \pm j\omega R_2C_{var}$  terms cancel out. Meanwhile, the group delay is mainly determined by the  $R_2C_{var}$  term. Cross-coupled differential pair with source degeneration capacitor  $C_0$  improves signal bandwidth.

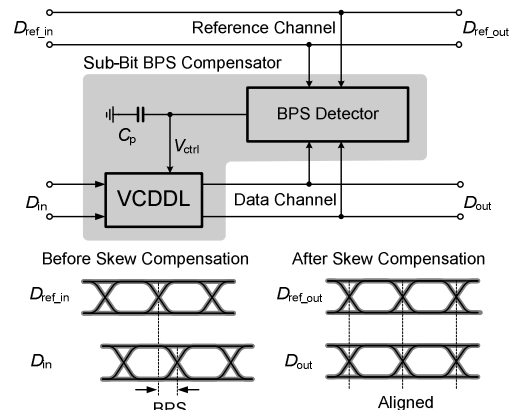


Fig. 1. Automatic sub-bit between-pair skew compensation scheme.

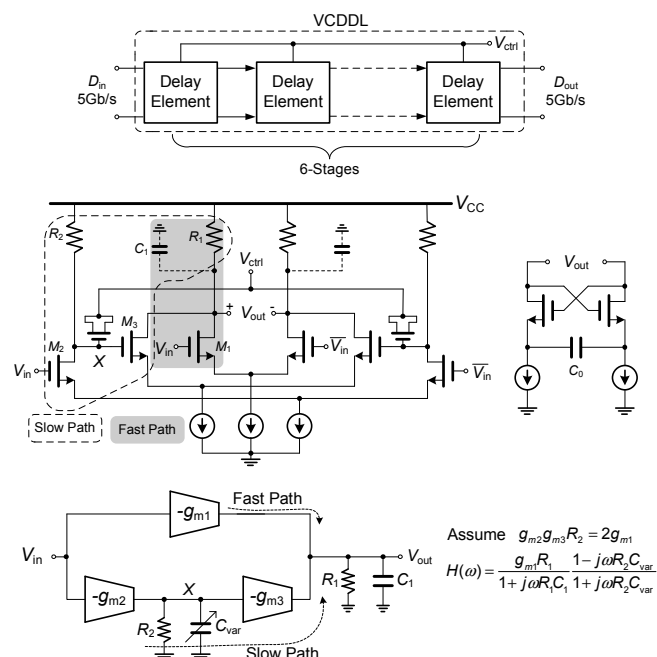


Fig. 2. VCDDL.

The skew detector needs to detect skew between two independent data sequences. Traditional phase detectors in PLL/DLL or CDR cannot be used here since they require at least one periodical input signal. Fig. 3 illustrates a partial skew detector, which is a key component of the complete BPS skew detector.  $V_A$  and  $V_B$  are two independent data sequences with same data rate and coding scheme, therefore, same UI and transition probability. Here,  $\tau$  is defined as the time difference between a particular transition point in  $V_A$  and the next transition point in  $V_B$ , assuming  $V_A$  is the reference. An edge detector, composed of an XOR gate and a delay cell, produces a  $\sigma$ -width pulse for each rising and falling edge. Then, an XNOR gate generates the partial skew detector output,  $I_{out}$ . The expected value of  $I_{out}$ ,  $E[I_{out}]$ , is a function of  $\tau$ , as illustrated. In the figure,  $\sigma$  is  $3UI/8$ . To achieve full sub-bit skew detection range,  $\sigma$  can be any value between  $UI/4$  and  $UI/2$ . During a UI time slot, there are four possible scenarios as shown in the figure. Here,  $P_{A1}$  ( $P_{B1}$ ) is the probability of “1” in streams  $V_{EA}$  ( $V_{EB}$ ) and is equal to the summation of the 1-to-0 and 0-to-1 transition probabilities of sequence  $V_A$  ( $V_B$ ).  $P_{A0}$  and  $P_{B0}$  are probabilities of opposite conditions.

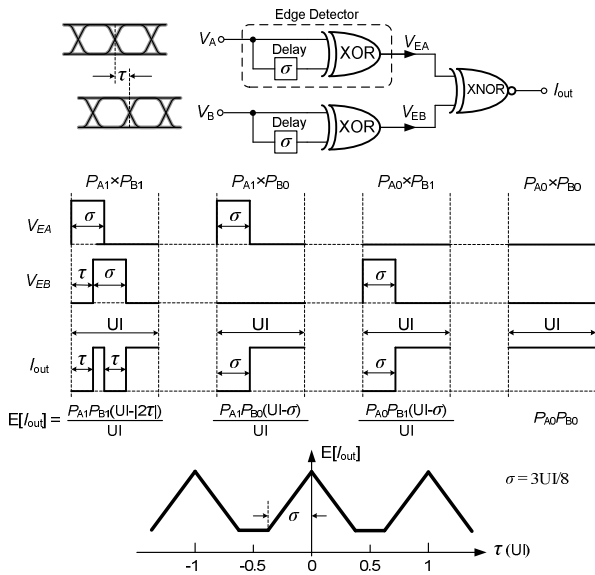


Fig. 3. Partial skew detector.

The partial skew detector output is always positive and symmetrical around  $\tau=0$ . However, the polarity of skew is required for correct skew compensation. Fig. 4 presents the proposed complete BPS detector incorporating two partial skew detectors with two additional delay cells, followed by a current subtraction circuit. The  $E[I_{ctrl}]$  value can identify the polarity of the skew. The XOR gates in the partial skew detector are implemented as modified Gilbert cells [6]. The XNOR gate and current subtraction circuits are shown.

### Measurement Results

A 5Gb/s BPS compensator was fabricated in  $0.13\mu\text{m}$  CMOS and the chip was wired bonded to a QFN-24 package. Fig. 5 is the chip micrograph. Fig. 6 shows measured reference channel and data channel signals before and after skew compensation for 100ps ( $UI/2$ ) BPS. These two signals are two unrelated  $2^{31}-1$  PRBS data. After skew compensation, signals of reference and data channels are successfully aligned as shown in both eye diagrams and transient captures. The BPS compensator, including the VCDDL and the BPS detector occupies  $0.03\text{mm}^2$  active die area and consumes 22.5mW.

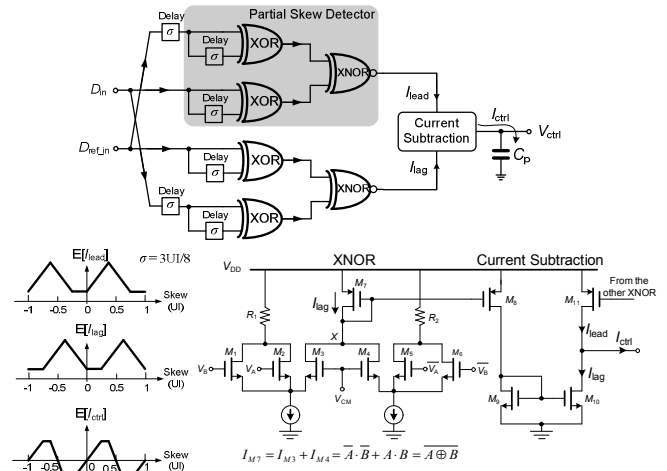


Fig. 4. BPS detector.

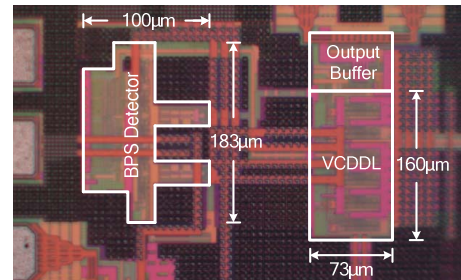


Fig. 5. Chip micrograph.

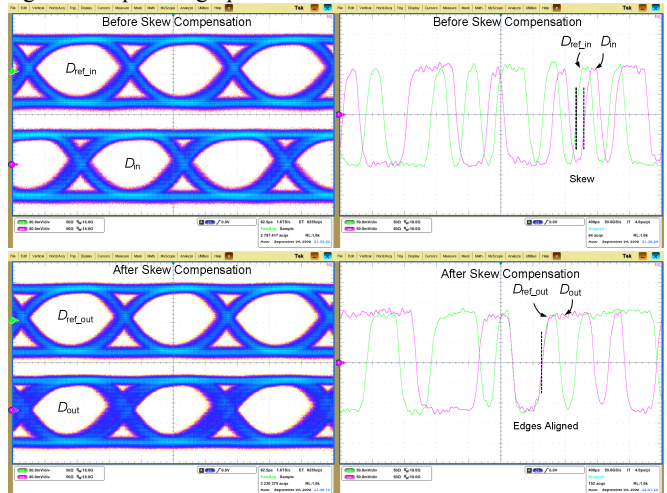


Fig. 6. Measured reference channel and data channel signals before and after skew compensation at 5Gb/s for 100ps BPS.

### References

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