

Qian Yu

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OBJECTIVE

To obtain a full-time position in Digital VLSI design

EXPERTISE

- VLSI System Design;
- Digital IC Design;
- Verification / Testing.

EDUCATION

- June 2006 **PhD E.E.:** VLSI System Design **GPA: 4.0**
Chinese Academy of Sciences
Dissertation Title: "Research and Design of Simultaneous Multithreading Micro-architecture"
- June 2001 **B.S. E.E.:** Communication Engineering **GPA: 3.9**
University of Science and Technology of China

EXPERIENCE

- Research of Processor's Micro-architecture *Mar. 2005-May 2006*
Analyzed the performance under real workloads of video applications to increase the throughput of the VLIW microprocessor and investigated SMT (Simultaneous Multithreading) micro-architecture which is an efficient method for quantities of vector operations and high thread-level parallelism in video CODEC applications.
- The Customized Design of a 16 Ports Register File Aug. 2004-Mar. 2005
Implemented a multi-ports register file which supported the high performance of the microprocessor. The design of scheme and layout in 500 MHz in 0.18 μ m CMOS technology has been accomplished. The utilized tools included HSPICE, CosmosSE, CosmosLE, Nanosim, StarRCXT.
- The Design of High Speed DSP&CPU Microprocessor Aug. 2003- Aug. 2004
Designed a microprocessor in 0.18 μ m CMOS technology, which was funded by a national project and speeded up to 266MHz with over one million gates. 1) Designed decoder and pipeline controller in VerilogHDL; 2) Verified the CPU core and SIMD coprocessor, as a manager of 4-person group. In the phase of verification, an efficient test-bench was built up to shorten the verification period; 3) Designed some kernel assembly programs for simulation. The chip got one-pass and ran an MPEG-2 decoding application as expected.
- The Customized Design of 6 Ports Register File in 400MHz Oct. 2002-Aug. 2003
Implemented the scheme and the layout of the register file as a small IP core in 0.18 μ m CMOS technology. Finished the optimization of the whole design. The utilized tools included HSPICE, CosmosSE, Enterprise, Star-sim, StarRC.
- The Design of Regular Multiplier Generator Mar. 2002-Oct. 2002
Designed the multiplier generator which can produce the RTL code under any parameter just like a small EDA tool. It was described in C++ language and synthesized in all widths to get the timing and area reports in Design-Compiler.

COMPUTER STILLS

Hardware Description Language: RTL Verilog and VHDL

Design tools: Synopsys, Mentor, Cadence, HSPICE, Matlab

Platforms: SUN, Unix, MS Windows, Linux

COURSES

VLSI Design;
Signal and System;

Digital System Engineering;
Communication Theory.

Computer Architecture;

AWARDS AND HONORS

- ✧ Excellent Graduate Student Scholarship, Graduate University of Chinese Academy of Sciences
- ✧ The Excellent Graduated Student of EE department, University of Science and Technology of China
- ✧ First Prize of Eastcom Scholarship, University of Science and Technology of China
- ✧ Second Prize of BELL in Shanghai Scholarship, University of Science and Technology of China
- ✧ Di'ao Scholarship in EE department, University of Science and Technology of China
- ✧ Third Prize of Excellent Undergraduate Student Scholarship, University of Science and Technology of China

LANGUAGE

Chinese /English bilingual

PUBLICATIONS

- Q. Yu, C.H. Hou, et al., "Fast Implementation of 2D DCT Based on Media Instructions", *Computer Engineering*, Jul. 2007. (accepted for publication)
- Q. Yu, C.H. Hou, et al., "Custom Design of 16-port Write-Through Memory Cell", *Microelectronic and Computers*, Dec. 2006. (accepted for publication)
- Q. Yu, C.H. Hou, et al., "A Design of 6-Port CMOS Register File", *Microelectronic and Computers*, Nov. 2005.
- Q. Yu, C.H. Hou, et al., "A Design of 500MHz 10-Read 6-Write Register File", in *Proceedings. 6th International Conference on ASIC*, Oct. 2005.
- Q. Yu, and D.H. Wang, "A Design of Regularized Multiplier Generator", in *Proceedings. 5th International Conference on ASIC*, Oct. 2003.