IBM: FinFET Isolation Considerations and Ramifications – Bulk vs. SOI

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Fully-depleted transistor technologies, both planar and fin-type, are now in the mainstream for product designs. One of the many interesting topics in the new 3D FinFET technology is the approach to isolation. In this article, key elements that differentiate junction-isolated (bulk) and dielectric-isolated (SOI) FinFET transistors are discussed, encompassing aspects of process integration, device design, reliability, and product performance.

Bulk vs. SOI basics

In bulk wafers, isolation is formed in a manner similar to planar devices, with implanted wells and shallow-trench-isolation oxide separating fins from one another.

With an SOI (silicon-on-insulator) wafer, however, the fins are formed in the silicon layer, the isolating dielectric is already extant, and no well implants are required.

Figure 1: Schematic representation of bulk junction and dielectric-isolated FinFETs

The most important differences in the devices formed in these two manifestations lie in the shape of the fin, the processes that determine the effective fin height, and the presence of doping, which consequently affects the device in many adverse ways such as the variability and the reliability.
The final realization of the full potential of fully-depleted FinFETs is dependent on optimally addressing the issues enumerated herein. Dielectric isolation is shown to provide superior characteristics in all of the above-named aspects. Figure 1 shows a schematic representation of FinFETs for the two isolation architectures, with the various critical points of distinction noted as are discussed below.

**Fin Shape**

Definition of the fins on an SOI wafer is relatively straightforward; vertical fin sidewalls may easily be obtained.

![Junction-isolated fin profile](Image)

![Dielectric-isolated fin profile](Image)

Figure 2: Typical bulk junction and dielectric-isolated FinFET fin profiles

In a bulk-based process, as the spaces between the lower, electrically inactive portions of the fins must be filled with an insulator, some angling of the fin is required to prevent the formation of voids.

Bulk and SOI fin profiles are pictured in Figure 2. As tapering the fin compromises the subthreshold slope and degrades the effective drive current as well as the output conductance, minimization of the taper is important to the electrical integrity of the device.

**Bulk: Doping in the Fin**

Whereas in an SOI design the transistor-transistor and subfin source-drain current paths are inherently interrupted by the dielectric layer, in a bulk-based process adequate doping for electrical isolation and latchup immunity needs to be established. This requires additional masking levels and connections for electrical bias.

Conventional design criteria of doping, depth, and overlay tolerances apply to the deep interdevice isolation wells, but suppression of undesired current in the drain-source region has unique features in the FinFET configuration.
Suppression of punchthrough current requires some level of doping at least in the bottom portion of the fin. The adverse effects of doping on mobility and random-dopant-fluctuation have been reported; non-uniform doping is particularly egregious as it increases capacitance without a concomitant increase in drive current.

However, the level of doping required depends on the alignment of the gate and the source junction depth. An optimum choice for the conjunction seeks to minimize the dopant required while respecting physical process window constraints (see Figure 3).

Figure 3: Short-channel effects as a function of doping and gate recess depth relative to the source junction depth in bulk FinFETs

Another adverse effect of doping in the fin is the implication for the gate work function. For junction-isolated FinFETs, the gate metal work function is established so as to provide the desired threshold voltage in the presence of doping; for undoped dielectric-isolated FinFETs the appropriate work function is closer to midgap, which reduces gate leakage and improves reliability.

Figure 4: Voltage operating range as a function of fin doping
Between RDF-driven \( V_{\text{min}} \) and work function-driven \( V_{\text{max}} \), the operating window of bulk FinFETs is more limited than that of undoped SOI FinFETs (see Figure 4).

**Product and Circuit Design Considerations**

Designing with planar bulk technology has historically differed from planar SOI technology in three aspects: well contacts, self-heating, and floating body effects.

At the expense of area, planar bulk technology has enjoyed the advantages of controlling the threshold voltage through the well potential. No such benefit exists in bulk FinFET devices, as it is not possible to influence the transistor through the well bias except in the spurious and undesirable region below the active fin.

In fully-depleted devices the concept of a floating body (charge storage in an isolated neutral region) is not applicable, so SOI and bulk FinFETs behave the same way for all switching scenarios.

Self-heating effects, while not important for fast switching operation, can be relevant for DC circuits. While large-area planar structures will continue enjoy the advantage in thermal conduction relative to SOI traditionally observed, bulk and SOI FinFETs have very similar self-heating characteristics, as the only difference in thermal conductance is a tall, thin sliver of silicon, which provides only a small increase in thermal conductance.

While bulk FinFET technology has lower soft error rates than planar bulk technology, SOI FinFETs are better yet.

**Variations**

Fin height variation has a much more serious impact than the planar analog of transistor width variation. Wide transistors (i.e., many fins) have the same variation as narrow (i.e., few fins).

Whereas in the SOI-based version the electrical fin height is determined by the starting silicon thickness, in the bulk-based FinFET process the fin height is determined by several processes, and the distinction between “active” and “inactive” fin is blurred by the conjunction of the gate alignment with the source junction.

The sensitivities to various key variables have been calculated with hardware-calibrated 3D simulations, and the variation of those key parameters determined with respect to state-of-the-art processes (see Figure 5).

The fin variation-driven performance tolerance of a bulk FinFET is larger than that of an SOI FinFET. That benefit of SOI is not only found in sort yield and worst-case design corners, but smaller variation within a chip enables a faster chip for any given level of leakage.
Figure 5: Calculated dependence of SOI and bulk transistors on key process variations, and relative variations in the two architectures

**Conclusion**

Complete realization of the benefits of fully-depleted transistor architecture is affected by the choice of isolation. Increased range of operating voltage, process simplification, reduced variation, lower soft error rate, and higher circuit density are all features of a dielectric-isolated architecture.

For these reasons the ability of an SOI-based FinFET to reap the full benefits of fully depleted transistors is demonstrably superior to a doped, bulk-based implementation.